avoid abandonment of the application. The objection to the drawings will not be held in abeyance." In response, Applicants have amended FIGs. 1-2B without adding new matter.

The Examiner rejected claims 1-6, 9-15 and 19-22 under 35 U.S.C. §102(b) as being unpatentable over McTeer (US 5,99,011). (Applicants believe the Examiner meant US 5,990,011).

The Examiner rejected claims 1-6, 9-15, 19-22 and 25-27 under 35 U.S.C. §102(e) as being unpatentable over Grill et al. (US 6,265,779 B1).

The Examiner rejected claims 1-6, 9-15, 19-22 and 25-27 under 35 U.S.C. §102(e) as being unpatentable over Farrar et al. (US 6,376,370 B1).

The Examiner rejected claims 7,8 16-18, 23, 24, 28 and 29 under 35 U.S.C. 103(a) as being unpatentable over Farrar (US 6,376,370B1) as applied to claims 1, 6, 10, 15, 20, 22, 25 and 27 above, and in further view of Havemann (US 6,156,651).

The Examiner rejected claims 30-33 under 35 U.S.C. 103 as being unpatentable over Farrar in view of Otsuka et al. (US 6,373,136 B2).

Applicants respectfully traverse the §102(b), §102(e) and §103 rejections with the following arguments.

35 USC § 102

As to claims 1, 10, and 20 the Examiner states that "Claims 1-6, 9-15, and 19-22 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by McTeer (US 5,99,011)."

Applicants contend that claims 1, 10 and 20, as amended, are not anticipated by McTeer because McTeer does not teach each and every feature of claims 1, 10 and 20.

In a first example, McTeer does not teach for claim 1, "at least a portion of the bottom of said upper level wire extending below the top surface of said dielectric layer", does not teach for

claim 10, "at least a portion of the bottom of said via extending below the top surface of said dielectric layer" and does not teach for claim 20 ", at least a portion of the bottom each via extending below the top surface of said dielectric layer."

In a second example, McTeer does not teach for claim 1 "said upper conductive liner in contact with said lower core conductor and also in contact with the inner surface or the outer surface or both the inner surface and the outer surface of said upper edge of said conductive liner", does not teach for claim 10 "said upper conductive liner on the bottom of said via in contact with said lower core conductor and also in contact with the inner surface or the outer surface or both the inner surface and outer surfaces of said upper edge of said lower conductive liner" and does not teach for claim 20 "each via of a second portion of said array of vias in contact with said lower core conductor and also in contact with the inner surface or the outer surface or both the inner surface and outer surface of said upper edge of said lower conductive liner."

Applicants respectfully point out in FIG. 3 of McTeer neither wetting layer 48 or second conductive layer 50 extend below the surface of first conductive layer 24 while in the applicants invention (see FIGs. 4A and more clearly FIG. 6A) upper conductive liner 225 clearly extends below the surface of lower level wire 200 and is embedded in lower conductive core 220. Applicants respectfully further point out that in FIG. 3 of McTeer, wetting layer 40 is in contact only with the top surface 32 of barrier layer 26 and not with the sides of barrier layer 26 while in the Applicants invention, see FIG. 4A and especially FIG. 4B and the description on page 19 lines 11-16, sides 290A and 290B of lower conductive liner 215 are contacting upper conductive liner 225.

Based on the preceding arguments, Applicants respectfully maintain that claims 1, 10 and 20 are not unpatentable over McTeer and are in condition for allowance. Since claims 2-4 and 6-

9 depend from claim 1, Applicants respectfully maintain that claims 2-4 and 6-9 are likewise in condition for allowance. Since claims 11-13 and 15-19 depend from claim 10, Applicants respectfully maintain that claims 11-13 and 15-19 are likewise in condition for allowance. Since claims 22-24 depend from claim 20, Applicants respectfully maintain that claims 22-24 are likewise in condition for allowance.

As to claims 1, 10, 20 and 25 the Examiner states that "1-6, 9-15, 19-22, and 25-27 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Grill et al. (US 6,265,779 B1)."

Applicants contend that claims 1, 10, 20 and 25, as amended, are not anticipated by Grill et al. because Grill et al. does not teach each and every feature of claims 1, 10, 20 and 25.

In a first example, Grill et al. does not teach for claim 1, "at least a portion of the bottom of said upper level wire extending below the top surface of said lower wire level", does not teach for claim 10 "at least a portion of the bottom of said via extending below the top surface of said lower wire level", does not teach for claim 20, " at least a portion of the bottom each via extending below the top surface of said lower wire level", and does not teach for claim 25, "at least a portion of the bottom each via extending below the top surface of said extensions of said lower wire level."

In a second example Grill et al. does not teach for claim 1, "said upper conductive liner in contact with said lower core conductor and also in contact with the inner surface or the outer surface or both the inner surface and outer surface of said upper edge of said conductive liner", does not teach for claim 10, "said upper conductive liner on the bottom of said via in contact with said lower core conductor and also in contact with the inner surface or the outer surface or both the inner surface and the outer surface of said upper edge of said lower conductive liner", does not teach for claim 20, "each via of a second portion of said array of vias in contact with said lower core conductor and also in contact with the inner surface or the outer surface or both

the inner surface and the outer surface of said upper edge of said lower conductive liner" and does not teach for claim 25, "said upper conductive liner on the bottom of each said via of a first portion of said array of vias in contact with said lower core conductor of said lower level wire and a second portion of said array of vias in contact with said lower core conductor of said extensions and also in contact with the inner surface or the outer surface or both the inner surface and the outer surface of said upper edge of said lower conductive liner of said extensions."

Applicants respectfully point out in all FIGs. of Grill et al. (taking FIG 2 as an example) liner 130 does not extend below the surface of wire 50 while in the applicants invention (see FIGs . 4A and more clearly FIG. 6A) upper conductive liner 225 clearly extends below the surface of lower level wire 200 and is embedded in lower conductive core 220. Applicants respectfully further point out that in FIG. 2A of Grill et al., liner 130 is in contact only with the top surface the liner of wire 50 and not with sides of the liner while in the Applicants invention, see FIG. 4A and especially FIG. 4B and the description on page 19 lines 11-16, sides 290A and 290B of lower conductive liner 215 are contacting upper conductive liner 225.

Further, in regards to claim 25, Grill does not teach "a lower level wire having a side and a bottom and one or more integral extensions each extension having a side and a bottom and extending laterally from the side of said lower level wire." Applicants respectfully point out that any feature that could be construed as a lateral extension of a wire is on the upper not lower wire and and these extensions do not contact any other wire in any other wire level. By contrast, Applicants FIGs. 12 and 13 clearly show the extension element 315(A/B/C of lower level wire 200 contacting the liner of the vias 210 formed in upper level wire 205.

Based on the preceding arguments, Applicants respectfully maintain that claims 1, 10, 20 and 25 are not unpatentable over Grill et al. and are in condition for allowance. Since claims 2-4 and 6-9 depend from claim 1, Applicants respectfully maintain that claims 2-4 and 6-9 are

likewise in condition for allowance. Since claims 11-13 and 15-19 depend from claim 10, Applicants respectfully maintain that claims 11-13 and 15-19 are likewise in condition for allowance. Since claims 22-24 depend from claim 20, Applicants respectfully maintain that claims 22-24 are likewise in condition for allowance. Since claims 27-29 depend from claim 25, Applicants respectfully maintain that claims 27-29 are likewise in condition for allowance.

As to claims 1, 10, 20 and 25 the Examiner states that "Farrar shows (fig. 3K) an interconnect structure comprising a lower level wire having a side and bottom, the lower level wiring comprising a core conductor (307B and 320) and a lower conductive liner (306B and 314)." Applicants can not find 320 in any FIG. of Farrar but have guessed it refers (in FIG. 3K) to the region boarded by 323, 321, and 382. The Examiner further states " The lower level wire also has integral extensions (part above 307), the extensions having a side and a bottom, wherein the lower level wire and extensions also comprise the lower core conductor (320) and the lower conductive liner (314). The liner is formed on the side and bottom of the lower level wire and the extension. The interconnect also comprises an upper level wire (330) having a side and bottom and a via integrally formed in the bottom of the upper level wire. The via also has a side and bottom. The upper level wire and via comprise an upper core conductor (344) and an upper conductive liner (334), which is formed on the side and bottom of the upper level wire and on the side and bottom of the via. The upper conductive liner on the bottom of the via is in contact with the lower core conductor and also in contact with the lower conductive liner in a liner-to-liner contact J. region. The lower level wire is formed in a lower level dielectric (302 and 308) and upper level wire is formed in an upper level dielectric (324). The upper and lower core conductors comprise copper (col. 17, lines 20-39) and the upper and lower conductive liners comprise tantalum nitride (col. 18, lines 22-23). The lower conductive liner includes an upper edge having an inner surface, an outer surface, and a top surface (top of layer 381 and 382) and

the upper conductive line on the bottom of the via contacts one of the top surfaces to form the liner-to-liner contact region. The liner-to-liner contact region also comprises a first portion co-extensive with the lower conductive liner on a portion of a first side (top surface of liner 314) of the lower level wire under the via (see the interface 319 between 383 and 381). The first and second dielectrics consist of silicon oxide (col. 17, lines 39-47)."

Applicants contend that claims 1, 10, 20 and 25, as amended, are not anticipated by Farrar because Farrar does not teach each and every feature of claims 1, 10, 20 and 25. In a first example, Farrar does not teach for claim 1,"at least a portion of the bottom of said upper level wire extending below the top surface of said lower wire level", does not teach for claim 10, "at least a portion of the bottom of said via extending below the top surface of said lower wire level", does not teach for claim 20, " at least a portion of the bottom each via extending below the top surface of said lower wire level", and does not teach for claim 25, "at least a portion of the bottom each via extending below the top surface of said extensions of said lower wire level."

In a second example Farrar does not teach for claim 1, "said upper conductive liner in contact with said lower core conductor and also in contact with the inner surface or the outer surface or both the inner surface and the outer surface of said upper edge of said conductive liner", does not teach for claim 10, "said upper conductive liner on the bottom of said via in contact with said lower core conductor and also in contact with the inner surface or the outer surface or both the inner surface and the outer surface of said upper edge of said lower conductive liner", does not teach for claim 20, "each via of a second portion of said array of vias in contact with said lower core conductor and also in contact with the inner surface or the outer surface or both the inner surface and the outer surface of said upper edge of said lower conductive liner" and does not teach for claim 25, "a second portion of said array of vias in contact with said lower core conductor of said extensions and also in contact with the inner

surface or the outer surface or both the inner surface and the outer surface of said upper edge of said lower conductive liner of said extensions."

First, Applicants respectfully point out that Farrar teaches in col. 15 lines 47 to 48 that layer 302 contains contact vias, teaches in col. 15, lines 62-66 that layer 308 contains a first level metal pattern and teaches in col. 18, lines 59-61 that layer 324 contains second level metal lines. Applicants contend, what Farrar is describing in FIG. 3K is the following: A layer 308 (containing wire containing a core 320 having liners 321, 316, 381 and 382) formed between a layer 324 (containing wire having a core 344 and liners 341, 336 384 and 383) and a layer 302 (containing a wire 307A/B having liners 306A/B). Therefore, there are three distinct wiring levels. Based on the preceeding, Applicants contend that the lower level wire can not comprise core conductors 307 and 320 because they are cores of separate wires and are separated by many intervening layers. Applicants also contend that the lower level wire is not formed in a lower dielectric (302 and 308), but rather one wire including core 320 is formed in layer 308 and another wire including core 302 is formed in layer 302.

Applicants respectfully point out in FIG. 3K of Farrar liner 383 does not extend below the surface of wire core 320 or layer 323 on top of conductor 320) nor does liner 381 extend below wire core 307A/B the while in the applicants invention (see FIGs. 4A and more clearly FIG. 6A) upper conductive liner 225 clearly extends below the surface of lower level wire 200 and is embedded in lower conductive core 220. Applicants respectfully further point out that in FIG. 3K of Farrar liner 383 is in contact only with the top surface the liners 881 and 382 and not with the sides of the liners nor is liner 381 in contact with the sides of liner 306A/B

Further, in regards to claim 25, Farrar does not teach "a lower level wire having a side and a bottom and one or more integral extensions each extension having a side and a bottom and extending laterally from the side of said lower level wire." The elements the Examiner contends

are "integral extension (part above 307) lower level extensions" are neither lateral extensions or integral or in contact with the upper wire. See Applicants discussion of Farrar FIG. 3K *supra*. It is patently clear that no portion of elements 320, 314, 382, 381, 321 or 316 is integral with any element in layer 302 or layer 324. The text of Farrar clearly indicates distinct and separate steps in forming these elements. Further, the examiner is indicating that the lower level wire comprises a core conductor 307B and 320 but layers 321, 316, 381 and 382 intervene so again the "extensions" can not be integral. By contrast, Applicants FIGs. 12 and 13 clearly show the extension element 315A/315B/315C of lower level wire 200 contacting the liner of the vias 210 formed in upper level wire 205 because the vias overlap sides 311A/B, 312A/B and 313A/B.

Based on the preceding arguments, Applicants respectfully maintain that claims 1, 10, 20 and 25 are not unpatentable over Farrar and are in condition for allowance. Since claims 2-4 and 6-9 depend from claim 1, Applicants respectfully maintain that claims 2-4 and 6-9 are likewise in condition for allowance. Since claims 11-13 and 15-19 depend from claim 10, Applicants respectfully maintain that claims 11-13 and 15-19 are likewise in condition for allowance. Since claims 22-24 depend from claim 20, Applicants respectfully maintain that claims 22-24 are likewise in condition for allowance. Since claims 27-29 depend from claim 25, Applicants respectfully maintain that claims 27-29 are likewise in condition for allowance.

35 USC § 103 Rejections

As to claims 30 and 31, the Examiner states that "Farrar shows (fig. 3K) an interconnect structure comprising a lower level wire having a side and bottom, the lower level wiring comprising a core conductor (307B and 320) and a lower conductive liner (3068 and 314). The liner is formed on the side and bottom of the lower level wire. The interconnect also comprises an upper level wire (330) having a side and bottom and a via integrally formed in the bottom of

the upper level wire. The via also has a side and bottom. The upper level wire and via comprise an upper core conductor (344) and an upper conductive liner (334), which is formed on the side and bottom of the upper level wire and on the side and bottom of the via. The upper conductive liner on the bottom of the via is in contact with the lower core conductor and also in contact with the lower conductive liner in a liner-to-liner contact J. region. The lower level wire is formed in a lower level dielectric (302 and 308) and upper level wire is formed in an upper level dielectric (324). Farrar shows all of the elements of the claims except the dielectric pillars formed in the lower level wire. Otsuka et al. discloses (col. 12, lines 30-52) insulating pillars formed in a level of wiring. With such a configuration a highly reliable damascene structure is formed (col. 2, lines 50-52). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the lower interconnect wiring level of Farrar by adding dielectric pillars as taught by Otsuka et al. to form a highly reliable damascene wiring structure."

Applicants contend that claim 30 is not obvious in view of Farrar in view of Otsuka et al. because Farrar in view of Otsuka et al. does not teach or suggest every feature of claim 30. As a first example, Farrar in view of Otsuka et al. does not teach or suggest "one or more dielectric pillars formed in said lower level wire, said lower conductive liner on sides of said dielectric pillars." As a second example, Farrar in view of Otsuka et al. does not teach or suggest "said upper conductive liner in contact with said lower core conductor and also in contact with said lower conductive liner on the sides of said dielectric pillars in liner-to-liner contact regions." Applicants respectfully point out that there is no liner mentioned in Otsuka et al. and in FIG. 13C to which col. 12, lines 30-52 refer, no interconnections between the wire (10) having pillars (P) and the other wire is (5) is illustrated or taught. Further Otsuka et al. consistently teaches forming connections between wiring levels (vias) away from the pillars (for example see FIG. 13A), thus teaching away from the invention. Further, the Examiner has stated that the urging to

combine the two references according to Otsuka et. al. is "to form a highly reliable damascene wiring structure." However, "highly reliable structure" according to Otsuka et al. means a structure with controlled grain size to avoid void formation, while the applicants invention does not avoid void formation but overcomes the effects of voids by liner-to liner contact. Thus there is no urging to combine references as the Examiner has asserted.

Based on the preceding arguments, Applicants respectfully maintains that claim 30 is not unpatentable over Fararr in view of Otsuka et al. and is in condition for allowance.

Applicants contend that claim 31 is not obvious in view of Farrar in view of Otsuka et al. because Farrar in view of Otsuka et al.does not teach or suggest every feature of claim 30. As a first example, Farrar in view of Otsuka et al. does not teach or suggest "one or more dielectric pillars formed in said lower level wire, said lower conductive liner on sides of said dielectric pillars." As a second example, Farrar in view of Otsuka et al. does not teach or suggest "at least a portion of said one or more vias in contact with said lower conductive liner on said side of at least a portion of said one or more dielectric pillars in liner-to-liner contact regions." Applicants respectfully point out that there is no liner mentioned in Otsuka et al. and in FIG. 13C to which col 12, lines 30-52 refer, no interconnections between the wire (10) having pillars (P) and the other wire is (5) is illustrated or taught. Further Otsuka et al. consistently teaches forming vias away from the pillars(for example, see FIG. 13A), thus teaching away from the invention. Further, the Examiner has stated that the urging to combine the two references is "to form a highly reliable damascene wiring structure." However according to Otsuka et al., "highly reliable structure" means a structure with controlled grain size to avoid void formation, while the applicants invention does not avoid void formation but overcomes the effects of voids by liner-to liner contact. Thus, there is no urging to combine references as the Examiner has asserted.

Based on the preceding arguments, Applicants respectfully maintains that claim 31 is not unpatentable over Fararr in view of Otsuka et al. and is in condition for allowance. Since claims 32-33 depend from claim 31, Applicants respectfully maintain that claims 32-33 are likewise in condition for allowance.

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that claims 1-4, 6-13, 15-20, 22-25, 27-35 meet the acceptance criteria for allowance and therefore request favorable action. If Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invite the Examiner to contact the Applicants' representative at the telephone number listed below.

Respectfully submitted,
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APPENDIX A - IDENTIFICATION OF AMENDED MATERIAL

Claims 1, 10, 20 and 25 are amended herein as follow:

1. (Once amended) An interconnect structure, comprising:

a lower level wire in a dielectric layer, said lower level wire having a side and a bottom, said lower level wire comprising a lower core conductor and a lower conductive liner, said lower conductive liner on the side and the bottom of said lower level wire, said lower conductive liner having an upper edge having an inner surface, an outer surface, and a top surface, the top surface of said upper edge substantially coplanar with a top surface of said dielectric layer;

an upper level wire having a side and a bottom, said upper level wire comprising an upper core conductor and an upper conductive liner, said upper conductive liner on the side and the bottom of said upper level wire, at least a portion of the bottom of said upper level wire extending below a top surface of said lower wire level; and

said upper conductive liner in contact with said lower core conductor and also in contact with the inner surface or the outer surface or both the inner surface and the outer surface of said upper edge of said conductive liner in a liner-to-liner contact region.

10. (Once amended) An interconnect structure, comprising:

a lower level wire in a dielectric layer, said lower level wire having a side and a bottom, said lower level wire comprising a lower core conductor and a[n] lower conductive liner, said lower conductive liner on the side and the bottom of said lower level wire, said lower conductive liner having an upper edge having an inner surface, an outer surface, and a top surface, the top surface of said upper edge substantially coplanar with a top surface of said dielectric layer;

an upper level wire having a side and a bottom and a via integrally formed in the bottom of said upper level wire, said via have a side and a bottom, said upper level wire and said via

each comprising an upper core conductor and an upper conductive liner, said upper conductive liner on the side and the bottom of said upper level wire and on the side and bottom of said via, at least a portion of the bottom of said via extending below a top surface of said lower wire level; and

said upper conductive liner on the bottom of said via in contact with said lower core conductor and also in contact with the inner surface or the outer surface or both the inner surface and the outer surface of said upper edge of said lower conductive liner in a liner-to-liner contact region.

20. (Once amended) An interconnect structure, comprising:

a lower level wire in a dielectric layer, said lower level wire having a side and a bottom, said lower level wire comprising a lower core conductor and a[n] lower conductive liner, said lower conductive liner on the side and the bottom of said lower level wire, said lower conductive liner having an upper edge having an inner surface, an outer surface, and a top surface, the top surface of said upper edge substantially coplanar with a top surface of said dielectric layer;

an upper level wire having a side and a bottom and an array of vias integrally formed in the bottom of said upper level wire, each via of said array of vias having a side and a bottom, said upper level wire and each via comprising an upper core conductor and an upper conductive liner, said upper conductive liner on the side and the bottom of said upper level wire and on the side and bottom of each via, at least a portion of the bottom each via extending below the top surface of said lower wire level; and

said upper conductive liner on the bottom of each via of a first portion of said array of vias in contact with said lower core conductor and each via of a second portion of said array of vias in contact with said lower core conductor and also in contact with the inner surface or the

outer surface or both the inner surface and the outer surface of said upper edge of said lower conductive liner in liner-to-liner contact regions.

25(Once amended) An interconnect structure, comprising:

a lower level wire in a dielectric layer, said lower level wire having a side and a bottom and one or more integral extensions each extension having a side and a bottom and extending laterally from the side of said lower level wire, said lower level wire and extensions comprising a lower core conductor and an lower conductive liner, said lower conductive liner on the side and the bottom of said lower level wire and said extensions, said lower conductive liner having an upper edge having an inner surface, an outer surface, and a top surface, the top surface of said upper edge substantially coplanar with a top surface of said dielectric layer;

an upper level wire having a side and a bottom and an array of vias integrally formed in the bottom of said upper level wire, each via of said array of vias having a side and a bottom, said upper level wire and each via comprising an upper core conductor and an upper conductive liner, said upper conductive liner on the side and the bottom of said upper level wire and on the side and bottom of each via, at least a portion of the bottom each via extending below a top surface of said extensions of said lower wire level; and

said upper conductive liner on the bottom of each said via of a first portion of said array of vias in contact with said lower core conductor of said lower level wire and a second portion of said array of vias in contact with said lower core conductor of said extensions and also in contact with the inner surface or the outer surface or both the inner surface and the outer surface of said upper edge of said lower conductive liner of said extensions in liner-to-liner contact regions.